# REMARKS

Applicants respectfully request the Examiner's reconsideration of the present application as amended.

Claims 1-25 are pending in the present application.

Claims 1-25 are rejected under 35 U.S.C. §102(e) as being unpatentable over U.S. Patent 6,782,511 ("Frank").

The Examiner has rejected claims 1-25 under 35 U.S.C. §102(e) as being unpatentable over Frank. In particular, the Examiner has stated that

> As to claim 1 Frank et al. teach a method for designing a system on a target device utilizing field programmable gate arrays (FPGA), comprising: identifying a group of components associated with a critical signal in the system (see fig 13 col 12 liens (sic) 1 to col 13 liens (sic) 18); creating a first copy and a second copy of the group of components where the first copy is driven by a first signal at a first state and the second copy is driven by a second signal at a second state (see fig 4, fig 8, fig 13 col 6 lines 54 to col 7 lines 27, and col 7 line 53 to col 10 lines 25); and configuring the system to select an output of one of the first copy and the second copy in response to the critical signal (see fig 8, fig 13 col 7 line 53 to col 10 lines 25 and background)

(2/24/2006 Office Action, p. 2)

It is submitted that Frank does not render claims 1-25 unpatentable under 35 U.S.C. §102(e).

Frank includes a disclosure of a business-to-business application service provider that includes an Internet website and webserver with EDA-on-demand solutions for system-on-a-chip designers. Such website allows electronic designs in hardware description language to be uploaded into a front-end EDA design environment. A behavioral model simulation tool hosted privately on the webserver tests and validates the design. Such tool executes only in the secure environment of the business-to-business application service provider. The validated solution is then downloaded back over the

Internet for a pay-per-use fee to the customer, and in a form ready to be placed and routed by a back-end EDA tool. Such validated design solutions are also downloadable to others in exchange for other designs, or available in technology libraries. The intellectual property created can be re-used, sold, shared, exchanged, and otherwise distributed efficiently and easily from a central for-profit clearinghouse. (see Frank Abstract).

It is submitted that Frank does not teach or suggest identifying a group of components associated with a critical signal in the system, creating a first copy and a second copy of the group of components where the first copy is driven by a first signal at a first state and the second copy is driven by a second signal at a second state, and configuring the system to select an output of one of the first copy and the second copy in response to the critical signal.

On the contrary, Frank discloses a step in technology mapping where a network graph 802 is partitioned into a collection of trees 804-808 or directed acyclic graphs (DAGs). The trees are defined so that their roots and leaves are all net nodes, as oppose to gate nodes. Root and leaf nodes are duplicated as many times as necessary (col. 7, lines 52-61, and Figure 8). Frank also discloses replacing logic trees with equivalent trees having no interior nodes and copying capacitive loads from leaves of a logic tree to leaves of a simplified tree (col. 6, lines 29-32, and 39-40 and Figure 3 block 306 and 314). Applicants submit that the root and leaf nodes that are duplicated with reference to Figure 8 and the logic trees and capacitive loads with reference to Figure 3 are not a group of components associated with a ***critical signal*** in the system. Moreover, applicants submit that a first copy and a second copy of the root and leaf nodes, logic tree, or capacitive loads are not created where the first copy is driven by a first signal at a first state and the second copy is driven by a second signal at a second state.

Furthermore, the Examiner cites column 12, lines 1 through column 13, line 18 as evidence that Frank discloses identifying a group of components associated with a critical signal in the system. Column 12, lines 1-16 describe Figure 8 which is a diagram of a circuit with critical-path signals shown in heavier lines. The critical signal propagation timing path extends between mux 1309, mux 1310, adder 1315, mux 1312, latch 1321, and latch 1320, adder 1316, and control FSM 1302. Applicants submit that none of these components are copied to create a first copy of a group of components and a second copy of the group of components where the first copy is driven by a first signal at a first state and the second copy is driven by a second signal at a second state.

Applicants further submit that the procedure in Frank which the Examiner cites as "identifying a group of components associated with a critical signal in the system" at columns 12 and 13 occurs ***after not before*** the procedures which the Examiner cites as "creating a first copy and a second copy of the group of components" disclosed at columns 6-10. Applicants request clarification of how Frank could disclose creating a first copy and a second copy of a group of components associated with a critical signal, before the group of components are identified.

In contrast, claim 1 states

> A method for designing a system on a target device utilizing field programmable gate arrays (FPGAs), comprising:
> identifying a group of components associated with a critical signal in the system;
> creating a first copy and a second copy of the group of components where the first copy is driven by a first signal at a first state and the second copy is driven by a second signal at a second state; and
> configuring the system to select an output of one of the first copy and the second copy in response to the critical signal.

(Claim 1) (Emphasis added).

Claims 10 and 19 include the limitation of duplicating components associated with a critical signal in the system. Given that claims 2-9, 11-18, and 21-25 depend directly or indirectly from claims 1, 10, and 19, it is likewise submitted that claims 2-9, 11-18, and 21-25 are also patentable under 35 U.S.C. §102(e) over Frank.

In view of the amendments and arguments set forth herein, it is respectfully submitted that the applicable rejections and have been overcome. Accordingly, it is respectfully submitted that claims 1-25 should be found to be in condition for allowance.

If any additional fee is required, please charge Deposit Account No. 50-1624.

Respectfully submitted,

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